Doc. Number:

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: N173DSE
SUFFIX: G31 Rev.C2

Customer: HP

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note
HP PN : 823423-7G2
HP HW : C2

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
3.0	July. 13, 2017	All	Spec Ver.3.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N173DSE-G31 is a 17.3” TFT Liquid Crystal Display module with LED Backlight unit and 40 pins eDP interface. This module supports 3840 x 2160 UHD mode and can display 16,777,216 colors.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	17.3” diagonal	-	-
Driver Element	a-si TFT active matrix	-	-
Pixel Number	3840 x R.G.B. x 2160	pixel	-
Pixel Pitch	0.09945 (H) x 0.09945 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	Hard coating (3H), High Resolution Adaptable AG (Haze 24%)	-	-
Color Gamut	Adobe 100%	NTSC	-
Luminance, White	300	Cd/m2	-
Power Consumption	Total (10.0) W (Max.) @ Cell (3.0) W (Max.), BL (7.0) W (Max.)		(1)

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	399.0	399.5	400.0	mm	(1) (2)
	Vertical (V)	229.95	230.45	230.95	mm	
	Vertical (V) with PCB & Bracket	243.4	243.9	244.4	mm	
	Thickness (T)	-	-	4.0	mm	
Polarizer Area	Horizontal	385.65	385.95	386.25	mm	-
	Vertical	218.15	218.35	218.55	mm	-
Active Area	Horizontal	381.79	381.89	381.99	mm	-
	Vertical	214.71	214.81	214.91	mm	-
Weight		-	520	550	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Dimensions are measured by caliper.

2.1 CONNECTOR TYPE

Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-040E-12.

User's connector Part No: IPEX-20453-040T-03.

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

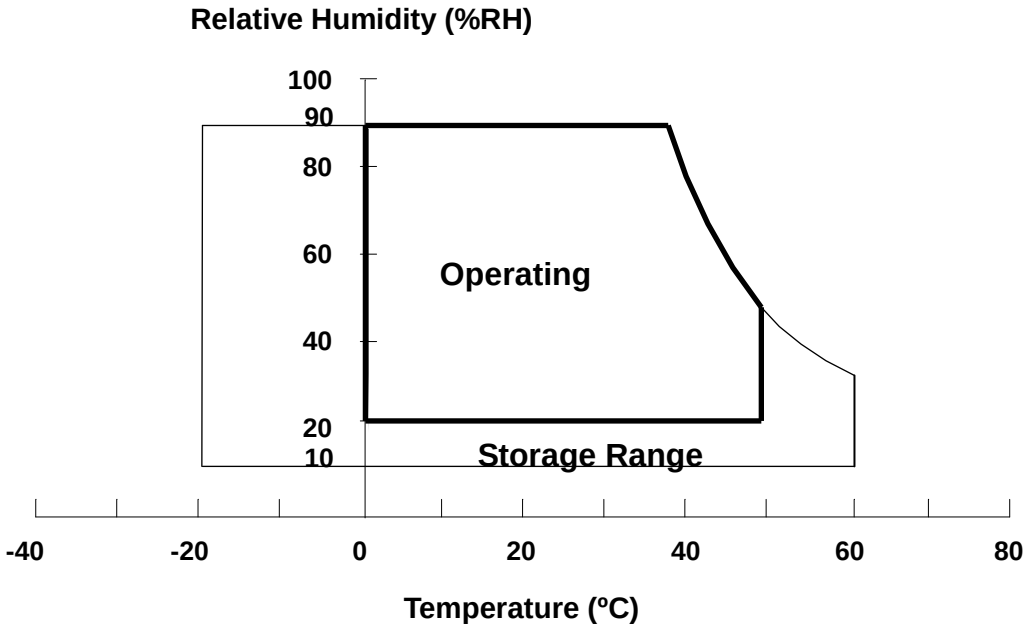
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta < 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

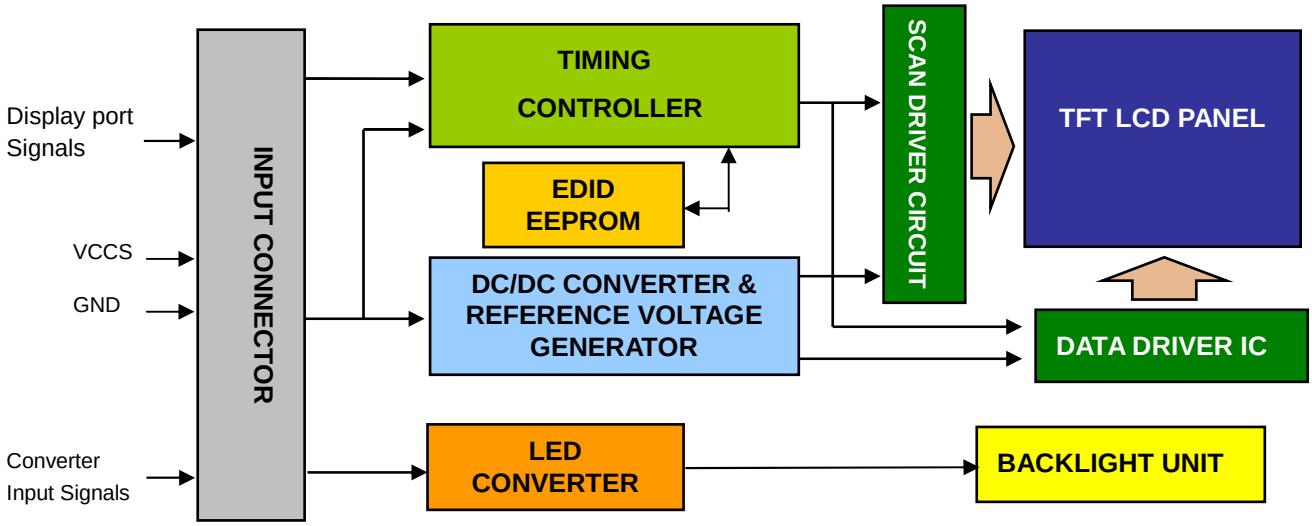
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	(26)	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	(5)	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	(5)	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



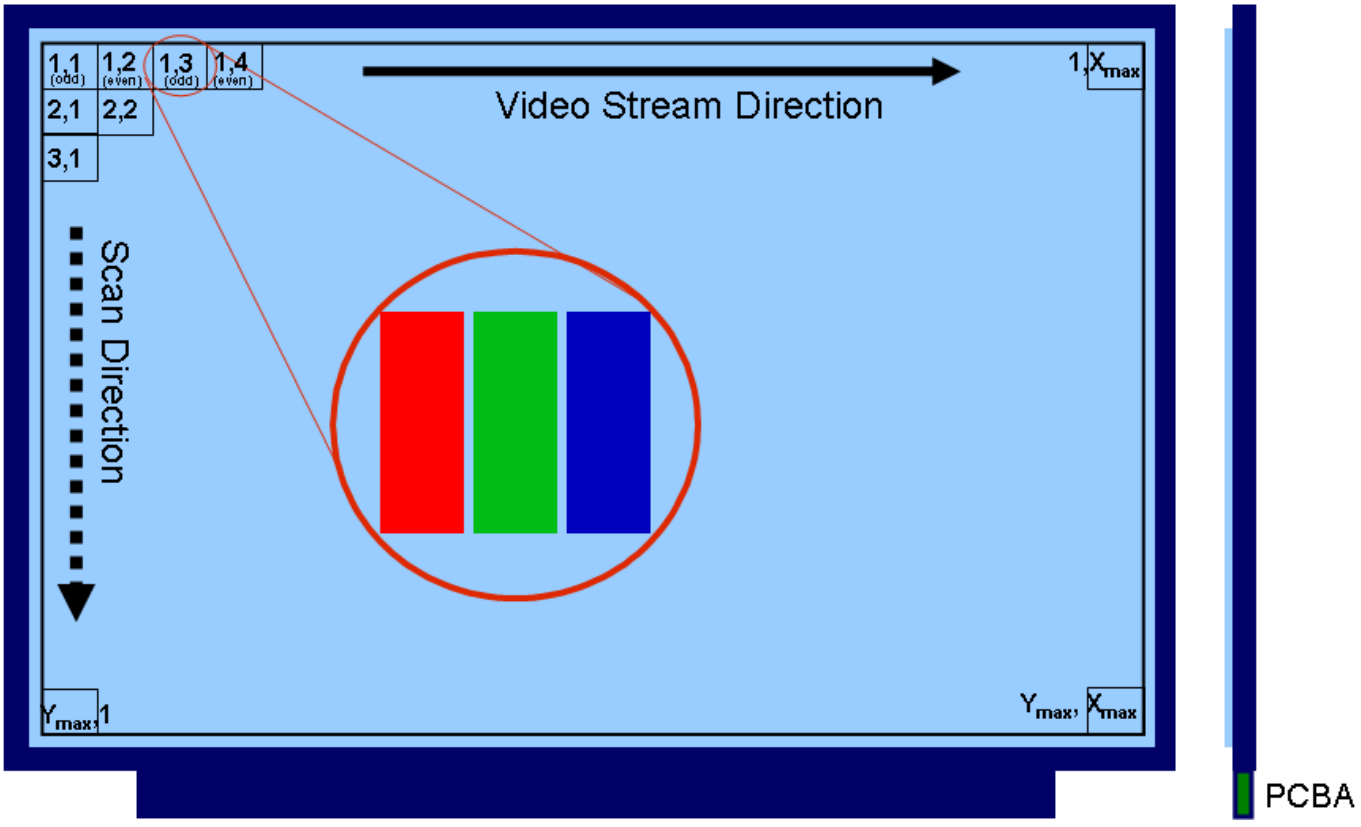
4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	-
2	H_GND	High Speed Ground	-
3	ML3-	Complement Signal-Lane 3	-
4	ML3+	True Signal-Main Lane 3	-
5	H_GND	High Speed Ground	-
6	ML2-	Complement Signal-Lane 2	-
7	ML2+	True Signal-Main Lane 2	-
8	H_GND	High Speed Ground	-
9	ML1-	Complement Signal-Lane 1	-
10	ML1+	True Signal-Main Lane 1	-
11	H_GND	High Speed Ground	-
12	ML0-	Complement Signal-Lane 0	-
13	ML0+	True Signal-Main Lane 0	-
14	H_GND	High Speed Ground	-
15	AUX+	True Signal-Auxiliary Channel	-
16	AUX-	Complement Signal-Auxiliary Channel	-
17	H_GND	High Speed Ground	-
18	VCCS	Power Supply +3.3 V (typical)	-
19	VCCS	Power Supply +3.3 V (typical)	-
20	VCCS	Power Supply +3.3 V (typical)	-
21	VCCS	Power Supply +3.3 V (typical)	-
22	NC	No Connection (Reserved for LCD test)	-
23	GND	Ground	-
24	GND	Ground	-
25	GND	Ground	-

26	GND	Ground	-
27	HPD	Hot Plug Detect	-
28	BL_GND	BL Ground	-
29	BL_GND	BL Ground	-
30	BL_GND	BL Ground	-
31	BL_GND	BL Ground	-
32	LED_EN	BL_Enable Signal of LED Converter	-
33	LED_PWM	PWM Dimming Control Signal of LED Converter	-
34	NC	No Connection (Reserved for LCD test)	-
35	NC	No Connection (Reserved for LCD test)	-
36	LED_VCCS	BL Power	-
37	LED_VCCS	BL Power	-
38	LED_VCCS	BL Power	-
39	LED_VCCS	BL Power	-
40	NC	No Connection (Reserved for LCD test)	-

Note (1) The first pixel is odd as shown in the following figure.



4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

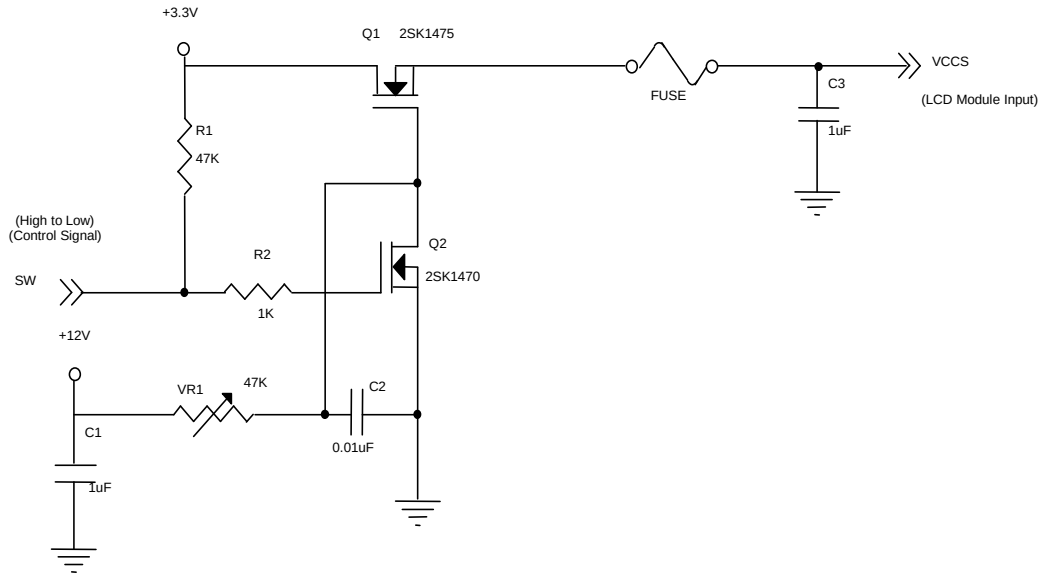
Parameter			Symbol	Value			Unit	Note
				Min.	Typ.	Max.		
Power Supply Voltage			VCCS	(3.0)	(3.3)	(3.6)	V	(1)
HPD		High Level	-	(2.25)	-	(2.75)	V	(5)
		Low Level	-	(0)	-	(0.4)	V	(5)
HPD Impedance			R_{HPD}	(30K)	-	-	ohm	(4)
Ripple Voltage			V_{RP}	-	(50)	-	mV	(1)
Inrush Current			I_{RUSH}	-	-	(1.5)	A	(1),(2)
Power Supply Current		Mosaic	Icc	-	(550)	(750)	mA	(3)a
		Black		-	(510)	(700)	mA	(3)

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

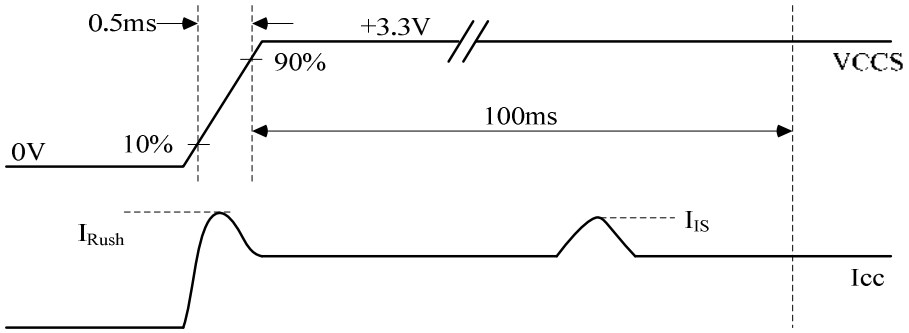
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

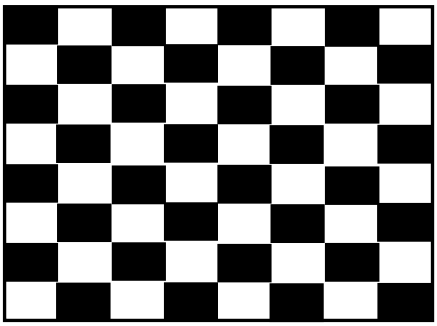


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (5) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action.

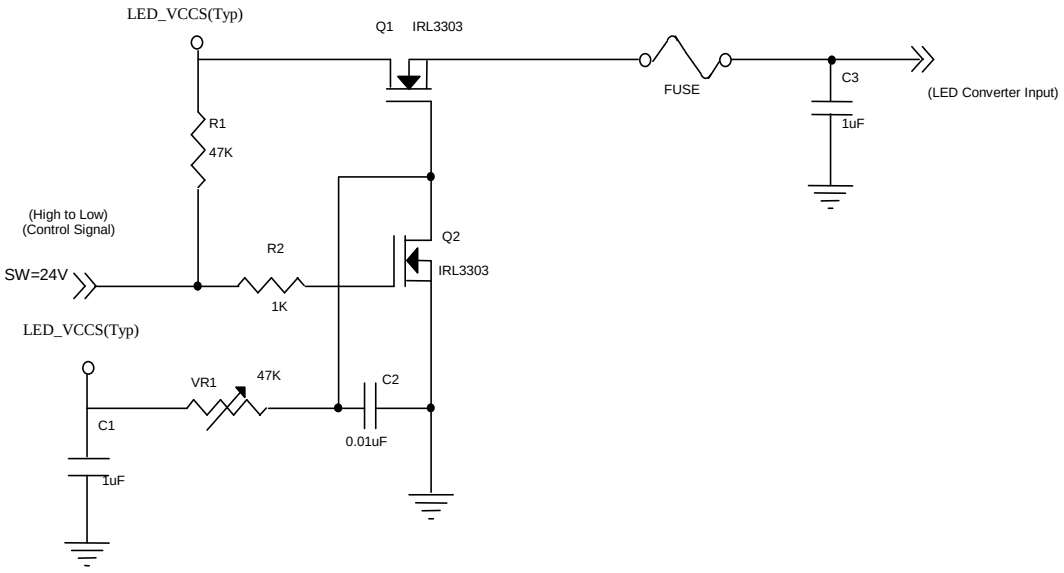
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	(8)	(12.0)	(20.0)	V	-
Converter Inrush Current		$ILED_{RUSH}$	-	-	(1.5)	A	(1)
LED_EN Control Level	Backlight On	-	(2.2)	-	(5)	V	(4)
	Backlight Off		(0)	-	(0.6)	V	(4)
LED_EN Impedance		R_{LED_EN}	(30K)	-	-	ohm	(4)
PWM Control Level	PWM High Level	-	(2.2)	-	(5)	V	(4)
	PWM Low Level		(0)	-	(0.6)	V	(4)
PWM Impedance			(30K)	-	-	ohm	(4)
PWM Control Duty Ratio			(5)	-	(100)	%	(5)
PWM Control Permissive Ripple Voltage		V_{PWM_pp}	-	-	(100)	mV	-
PWM Control Frequency		f_{PWM}	(190)	-	(2K)	Hz	(2)
LED Power Current	LED_VCCS =Typ.	ILED	(484)	(578)	(584)	mA	(3)

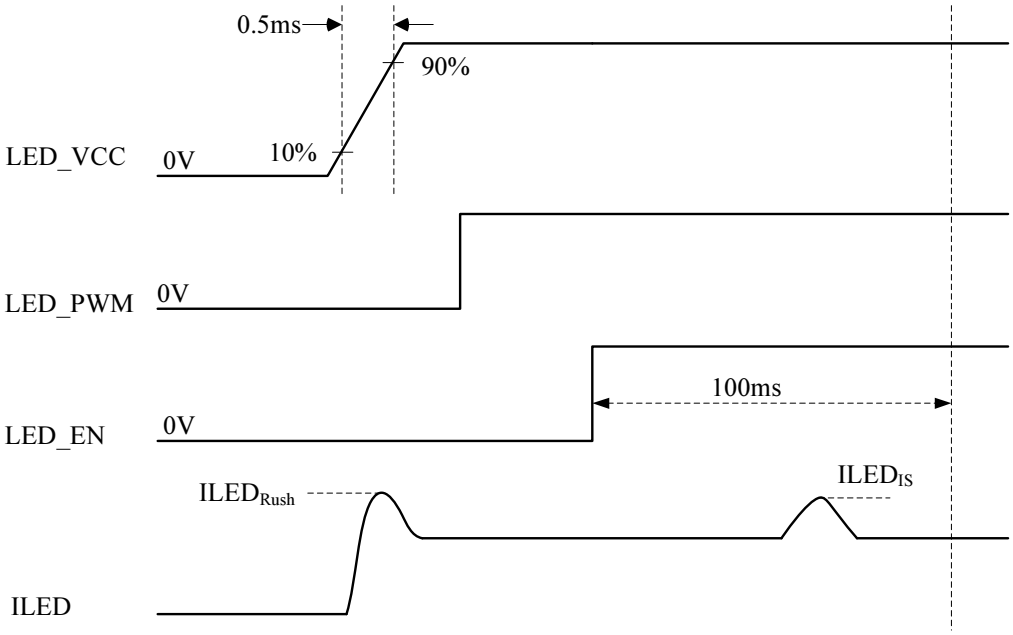
Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

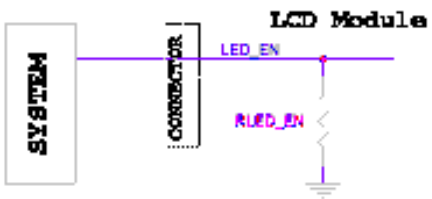
$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer $(N \geq 3)$

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (If it exists). The rest pull down impedances of other signals (eg. HPD, PWM …) are in the same concept.



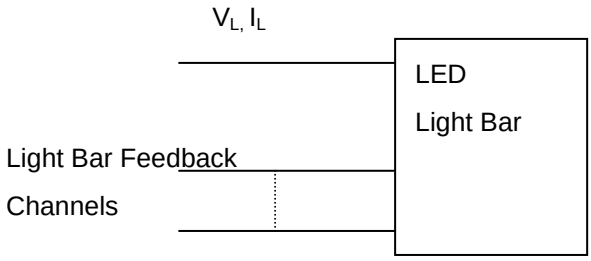
Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	28.6	31.9	33.0	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	-	187.2	-	mA	
Power Consumption	P_L	-	5.971	6.177	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 ^oC and I_L = 23.4 mA (Per EA) until the brightness becomes $\leqq$ 50% of its original value.

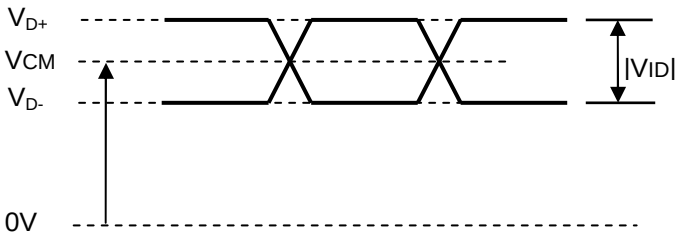
4.4 DISPLAY PORT SIGNAL TIMING SPECIFICATION

4.4.1 DISPLAY PORT INTERFACE

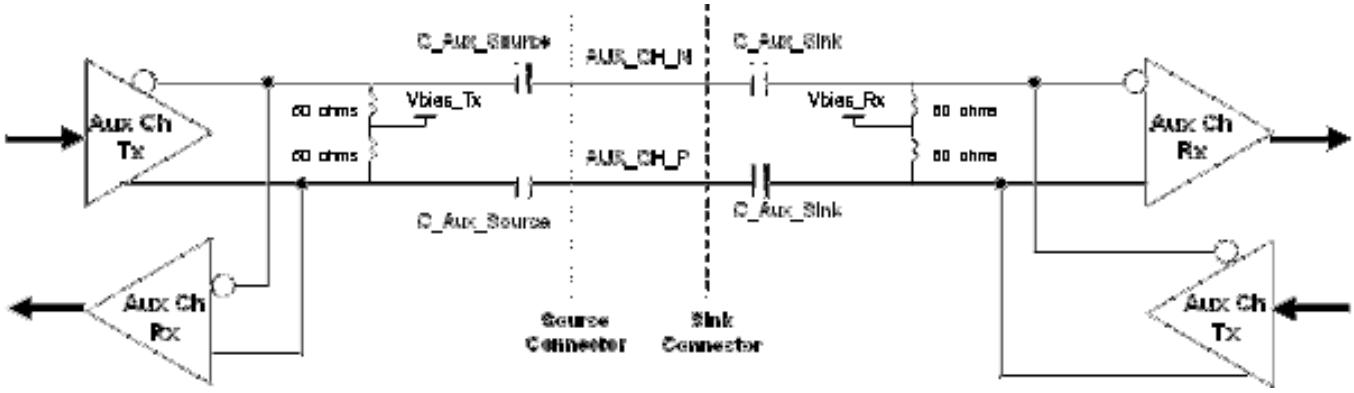
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0	-	2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75	-	200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75	-	200	nF	(3)

Note (1) Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.3. If some optional item is requested, please contact us.

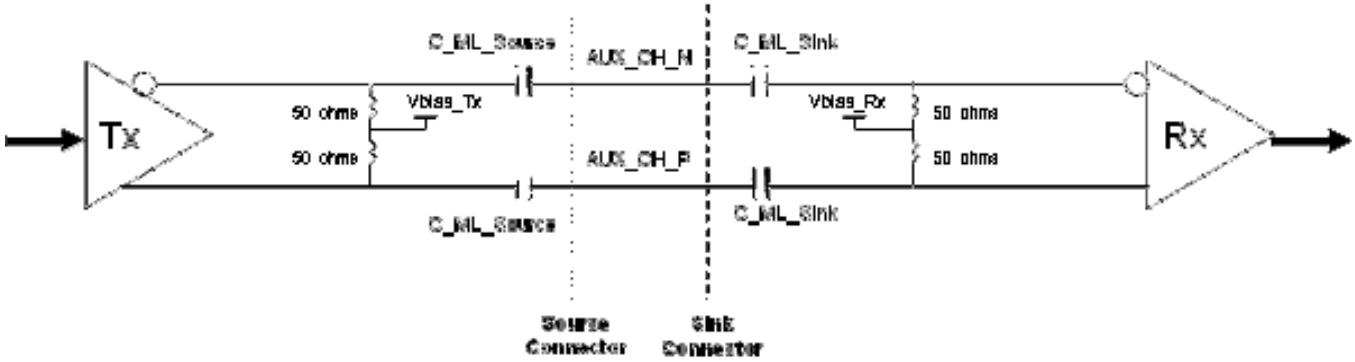
Single Ended



Note (2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



Note (3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



Note (4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1.

4.4.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

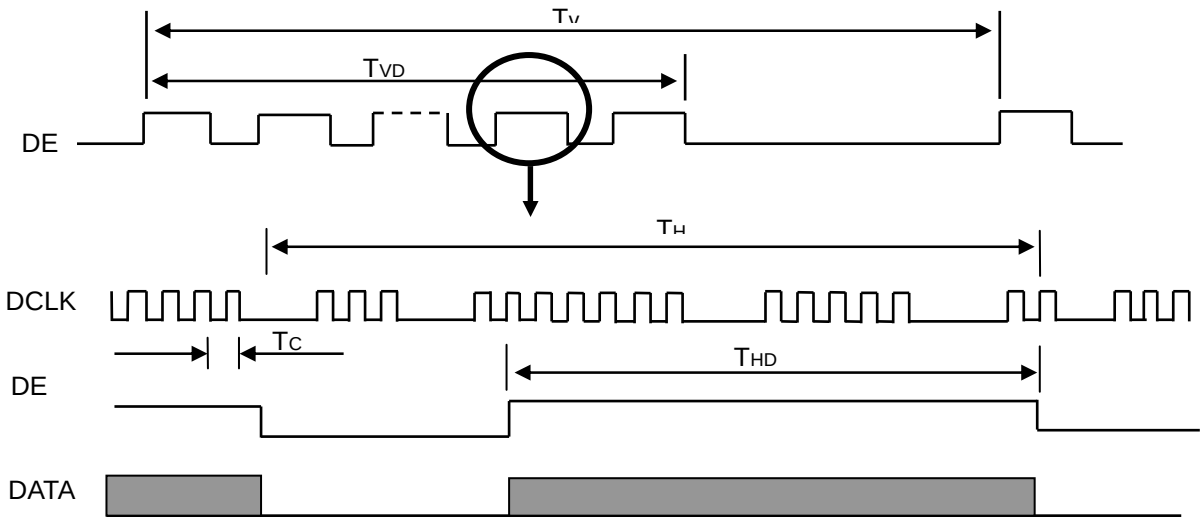
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram**.**

Refresh rate 60Hz

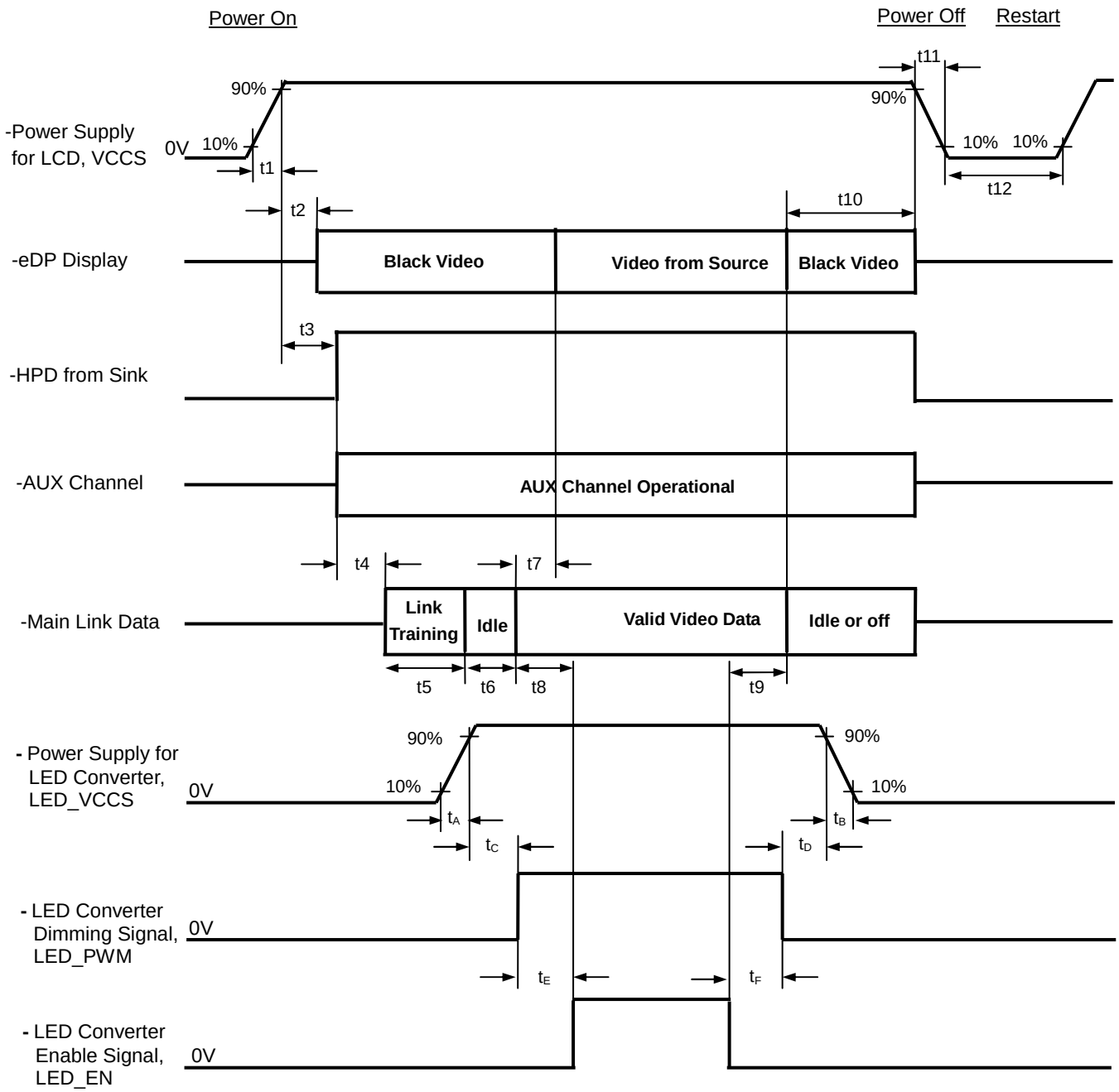
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	(530.61)	(533.28)	(535.94)	MHz	-
DE	Vertical Total Time	TV	(2175)	(2222)	(2237)	TH	-
	Vertical Active Display Period	TVD	(2160)	(2160)	(2160)	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	(62)	TV-TVD	TH	-
	Horizontal Total Time	TH	(3970)	(4000)	(4040)	Tc	-
	Horizontal Active Display Period	THD	(3840)	(3840)	(3840)	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	(160)	TH-THD	Tc	-

INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram**.**



Timing Specifications:

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	(0.5)	(10)	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	(0)	(200)	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	(0)	(200)	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	(0)	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	(0)	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	(0)	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	(0)	(50)	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	(80)	-	ms	Source must assure display video is stable
t9	Delay from backlight off to end of valid video data	Source	(50)	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below)
t10	Delay from end of valid video data from Source to power off	Source	(0)	(500)	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	(0.5)	(10)	ms	-
t12	VCCS Power off time	Source	(500)	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	(0.5)	(10)	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	(0)	(10)	ms	-

t_C	Delay from LED power rising to LED dimming signal	Source	(1)	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	(1)	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	(0)	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	(0)	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max. The panel's HPD may go high following LCDVCC(VCCS) power-on and goes low within 10ms, then the HPD stays low longer than 2ms. So, it must be regarded as a Hot-Plug/Unplug-Event. According to Section 5.1.4 of "VESA DisplayPort Standard", the source must read the link / sink status field and receiver capability field of the DPCD and re-train the link.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

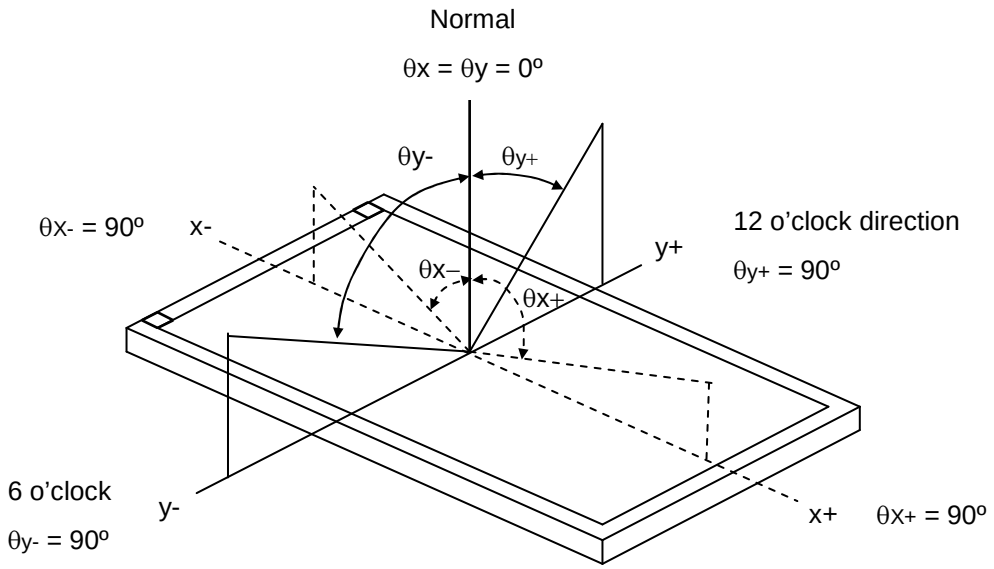
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	187.2	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	700	1000	-	-	(2), (5) ,(7)
Response Time		T_R		-	14	17	ms	(3) ,(7)
		T_F		-	16	18	ms	
Average Luminance of White		L_{AVE}		255	300	-	cd/m^2	(4), (6) ,(7)
Color Chromaticity	Red	Rx		Typ – 0.03	(0.640)	Typ + 0.03	-	(1) ,(7)
		Ry			(0.330)		-	
	Green	Gx			(0.210)		-	
		Gy			(0.710)		-	
	Blue	Bx			(0.150)		-	
		By			(0.060)		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	80	89	-	Deg.	(1),(5) , (7)
		θ_x-		80	89	-		
	Vertical	θ_Y+		80	89	-		
		θ_Y-		80	89	-		
White Variation		δW_{5p}	θ_x=0°, θ_Y =0°	-	-	1.25	%	(5),(6) , (7)
		δW13p	θx=0°, θY =0°	-	1.4	1.6	%	(5),(6) , (7)

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

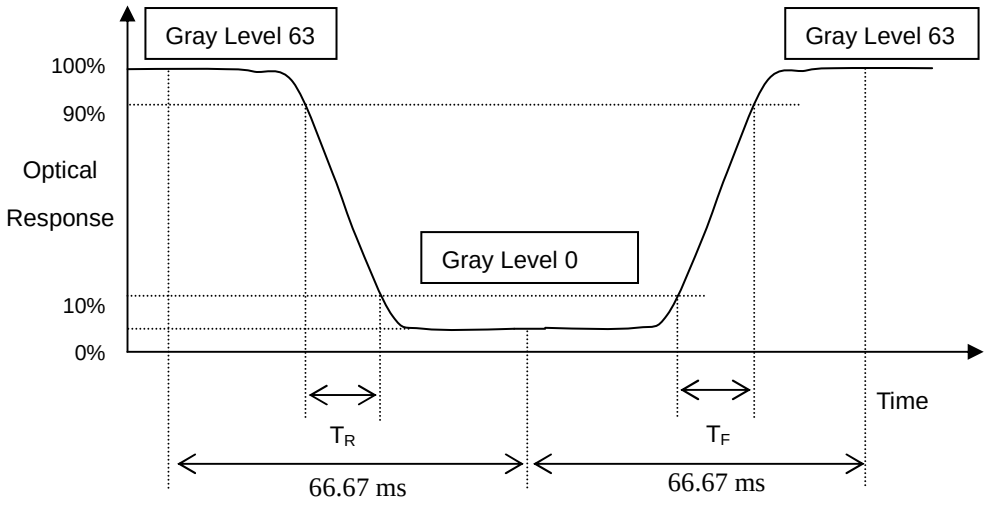
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

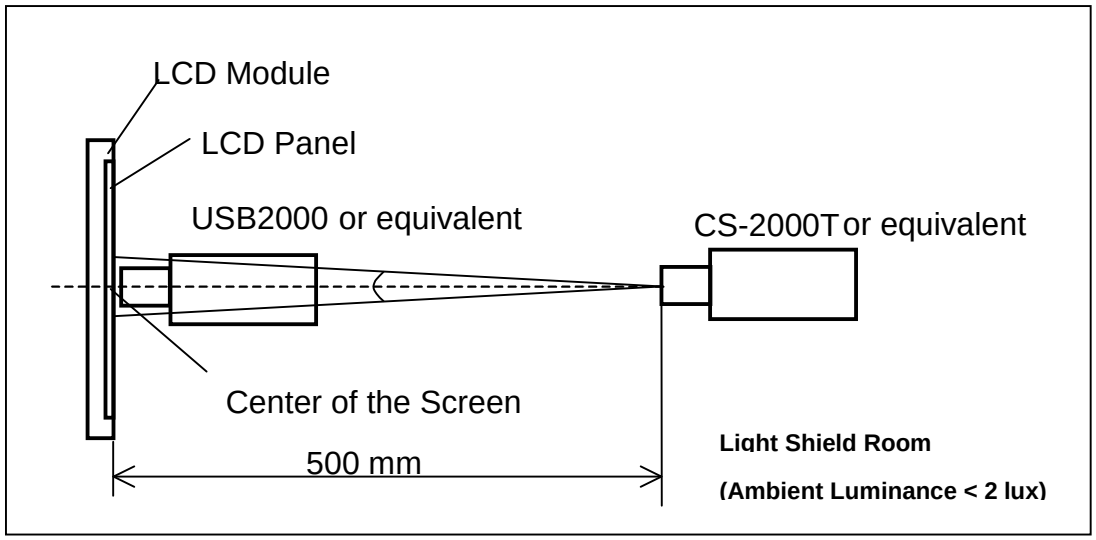
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

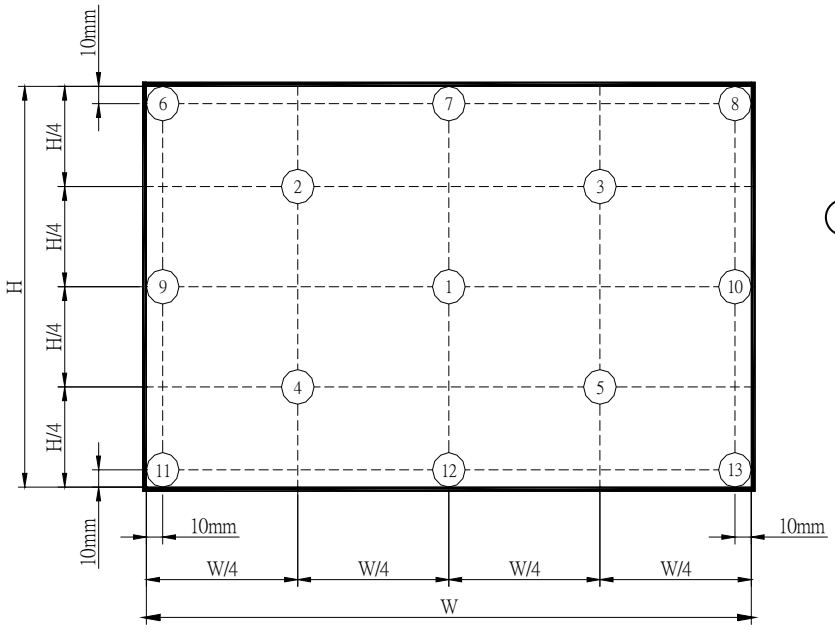


Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW_{5p} = {Maximum [L (1) ~ L (5)] / Minimum [L (1) ~ L (5)]}*100%

δW_{13p} = {Maximum [L (1) ~ L (13)] / Minimum [L (1) ~ L (13)]} *100%



X : Test Point

X=1 to 13

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50ºC, RH 80%, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria: Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

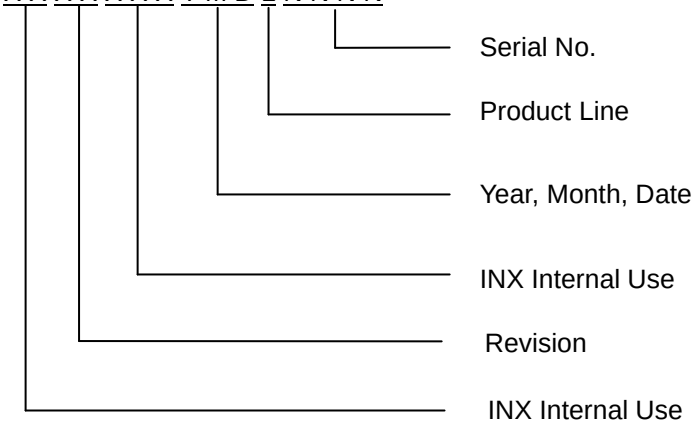
7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N173DSE – G31

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N



(d) Production Location: MADE IN XXXX.

(e) UL Logo：XXXX or XXXXX is UL factory ID.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

CT Label

S/N	CT: CGAPHRRXXWWXXX
CT:	Title
C	LCD Display Module
GAPH	Assembly Code
RR	Revision
XX	Supplier /Site of MFG
WW	Week/Year of MFG
XXX	Serial number. From 000000 to 999999

7.2 CARTON

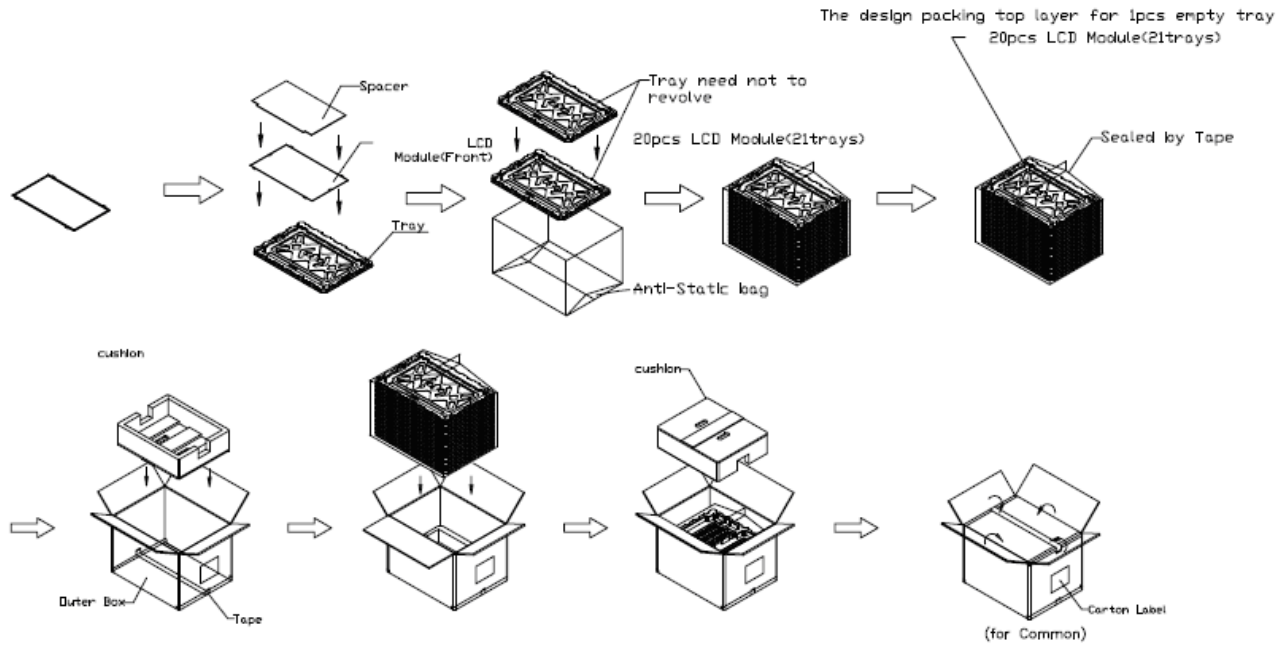


Figure. 7-1 Packing method

7.3 PALLET

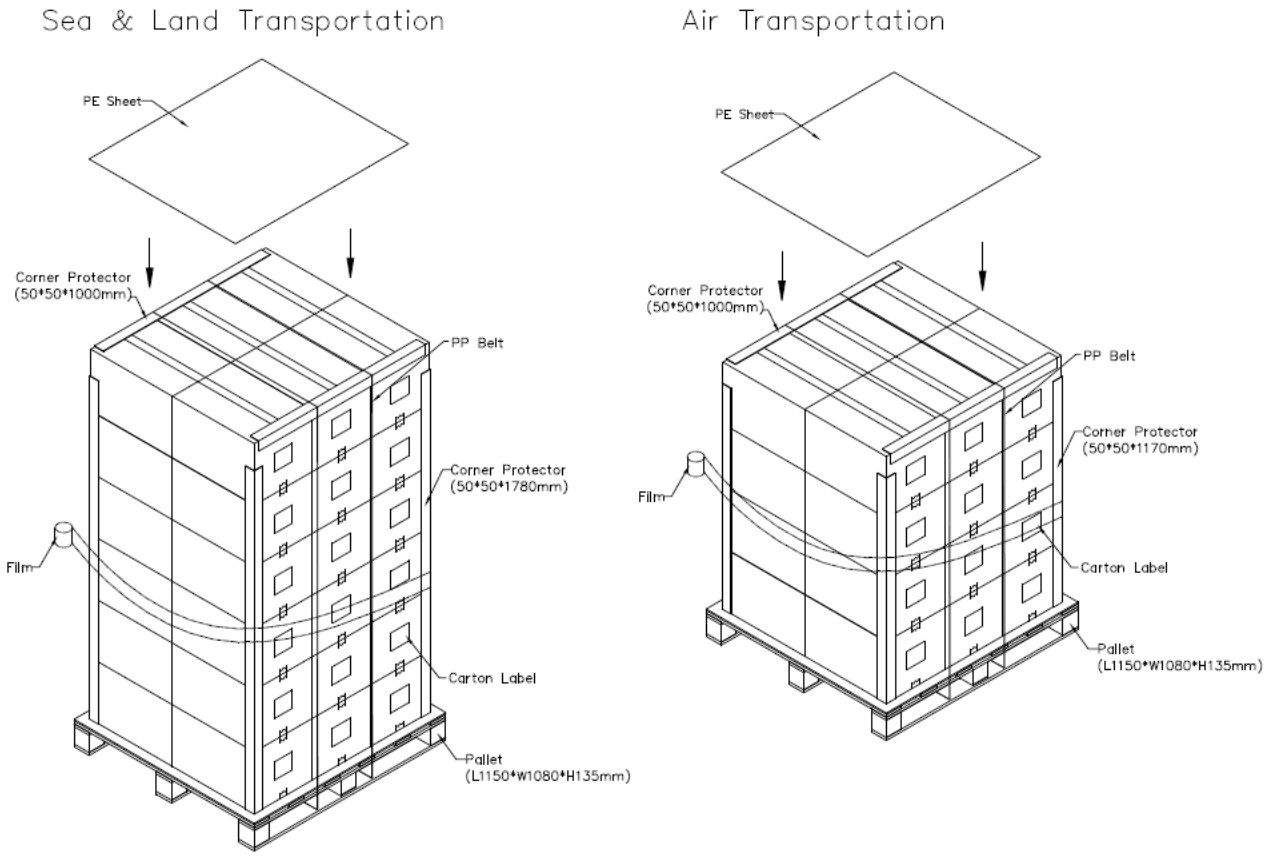


Figure. 7-2 Packing method

7.4 UN-PACKAGING METHOD

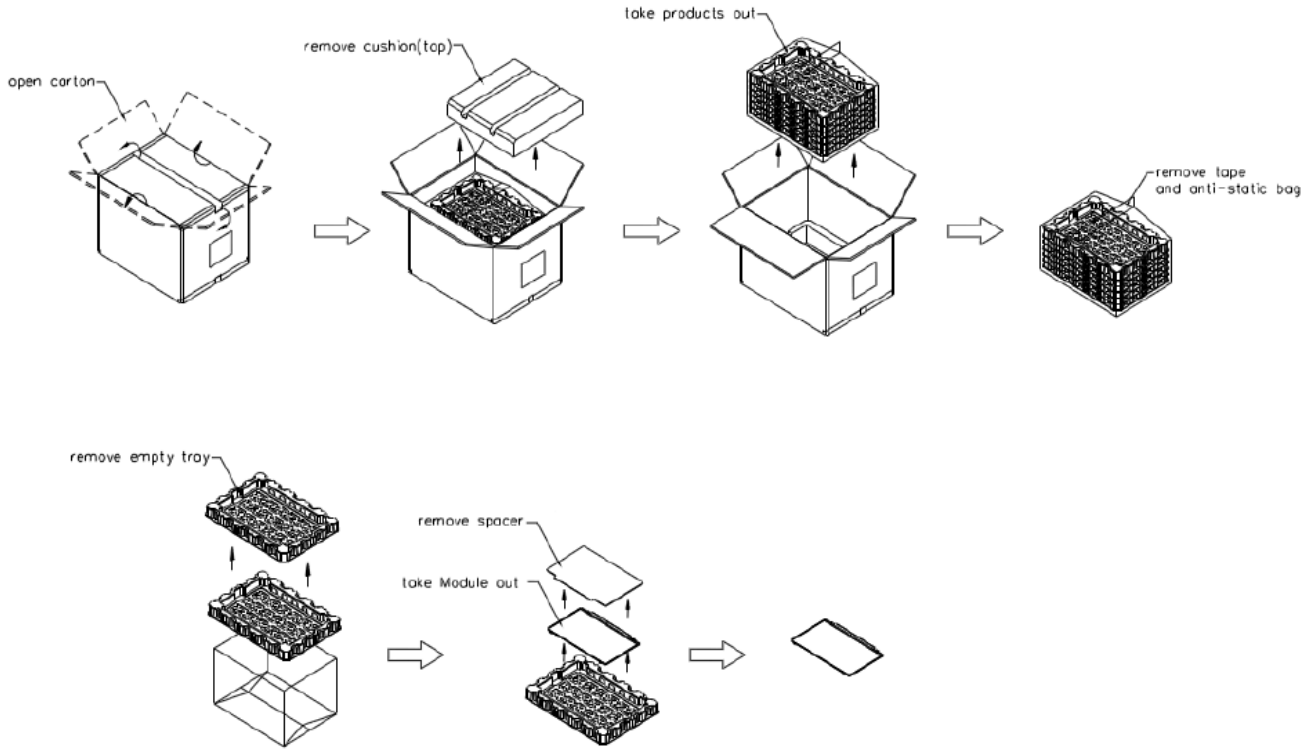


Figure. 7-3 Un-Packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

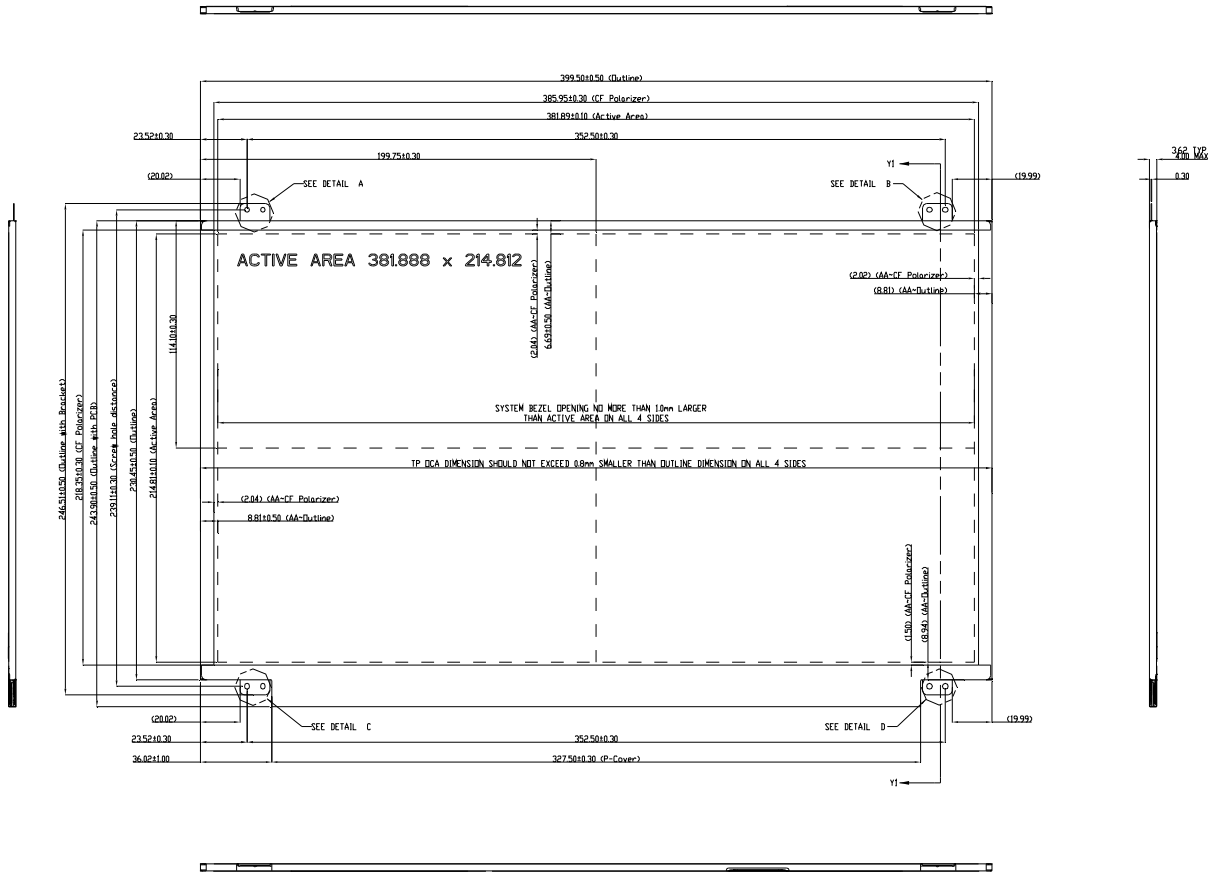
The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

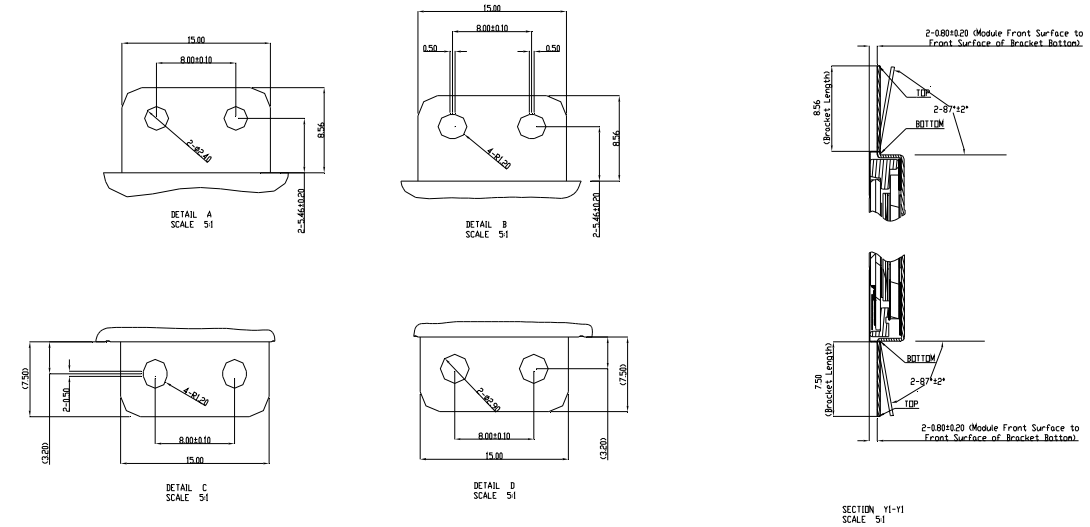
Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	EISA ID manufacturer name ("CMN")	0D	00001101
9	09	EISA ID manufacturer name	AE	10101110
10	0A	ID product code (LSB)	43	01000011
11	0B	ID product code (MSB)	17	00010111
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	16	00010110
17	11	Year of manufacture (fixed year code)	19	00011001
18	12	EDID structure version ("1")	01	00000001
19	13	EDID revision ("4")	04	00000100
20	14	Video I/P definition ("Digital")	A5	10100101
21	15	Active area horizontal (“38.1888cm“)	26	00100110
22	16	Active area vertical (“21.4812cm“)	15	00010101
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB, Non-continous")	02	00000010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	EF	11101111
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	95	10010101
27	1B	Rx=0.64	A3	10100011
28	1C	Ry=0.33	54	01010100
29	1D	Gx=0.21	35	00110101
30	1E	Gy=0.71	B5	10110101
31	1F	Bx=0.15	26	00100110
32	20	By=0.06	0F	00001111
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

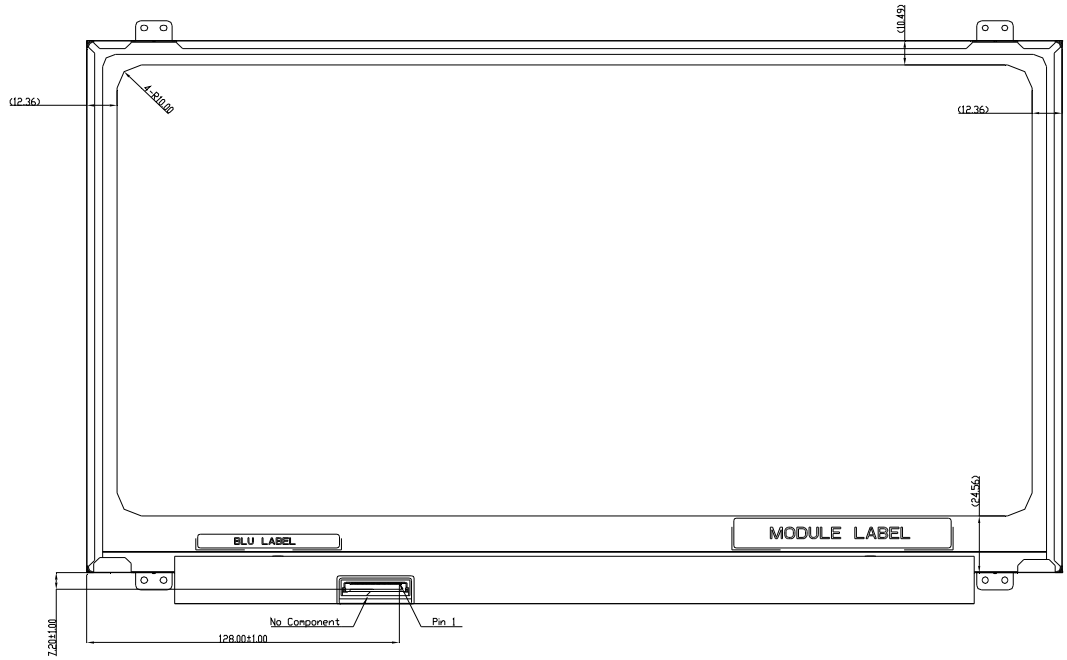
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("533.28"MHz, According to VESA CVT Rev1.4)	50	01010000
55	37	# 1 Pixel clock (hex LSB first)	D0	11010000
56	38	# 1 H active ("3840")	00	00000000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank ("3840 : 160")	F0	11110000
59	3B	# 1 V active ("2160")	70	01110000
60	3C	# 1 V blank ("62")	3E	00111110
61	3D	# 1 V active : V blank ("2160 : 62")	80	10000000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 5")	35	00110101
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48 : 32 : 3 : 5")	00	00000000
66	42	# 1 H image size (“381 mm“)	7D	01111101
67	43	# 1 V image size (“214 mm“)	D6	11010110
68	44	# 1 H image size : V image size	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
72	48	Detailed timing description # 2 Pixel clock ("533.28"MHz, According to VESA CVT Rev1.4)	50	01010000
73	49	# 2 Pixel clock (hex LSB first)	D0	11010000
74	4A	# 2 H active ("3840")	00	00000000
75	4B	# 2 H blank ("160")	A0	10100000
76	4C	# 2 H active : H blank ("3840 : 160")	F0	11110000
77	4D	# 2 V active ("2160")	70	01110000
78	4E	# 2 V blank ("506")	FA	11111010
79	4F	# 2 V active : V blank ("2160 : 506")	81	10000001
80	50	# 2 H sync offset ("48")	30	00110000
81	51	# 2 H sync pulse width ("32")	20	00100000
82	52	# 2 V sync offset : V sync pulse width ("3 : 5")	35	00110101
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width ("48 : 32 : 3 : 5")	00	00000000
84	54	# 2 H image size (“381 mm“)	7D	01111101
85	55	# 2 V image size (“214 mm“)	D6	11010110

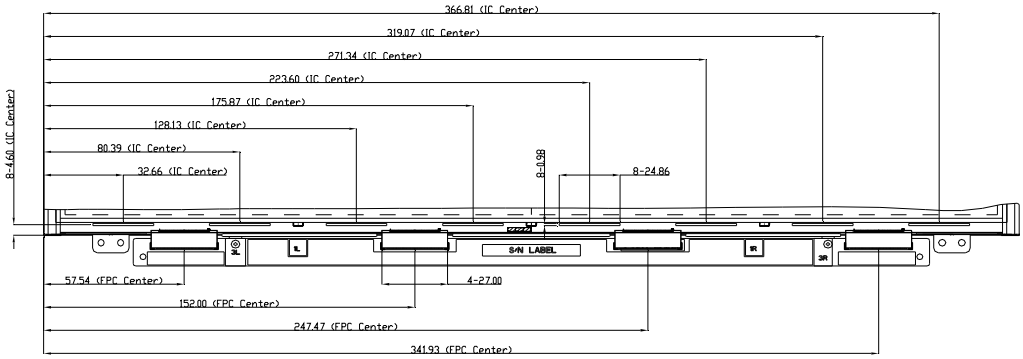
86	56	# 2 H image size : V image size	10	00010000
87	57	# 2 H boarder ("0")	00	00000000
88	58	# 2 V boarder ("0")	00	00000000
89	59	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
90	5A	Detailed timing description # 3 Pixel clock ("533.28"MHz, According to VESA CVT Rev1.4)	50	01010000
91	5B	# 3 Pixel clock (hex LSB first)	D0	11010000
92	5C	# 3 H active ("3840")	00	00000000
93	5D	# 3 H blank ("160")	A0	10100000
94	5E	# 3 H active : H blank ("3840 : 160")	F0	11110000
95	5F	# 3 V active ("2160")	70	01110000
96	60	# 3 V blank ("617")	69	01101001
97	61	# 3 V active : V blank ("2160 : 617")	82	10000010
98	62	# 3 H sync offset ("48")	30	00110000
99	63	# 3 H sync pulse width ("32")	20	00100000
100	64	# 3 V sync offset : V sync pulse width ("3 : 5")	35	00110101
101	65	# 3 H sync offset : H sync pulse width : V sync offset : V sync width ("48 : 32 : 3 : 5")	00	00000000
102	66	# 3 H image size (“381 mm“)	7D	01111101
103	67	# 3 V image size (“214 mm“)	D6	11010110
104	68	# 3 H image size : V image size	10	00010000
105	69	# 3 H boarder ("0")	00	00000000
106	6A	# 3 V boarder ("0")	00	00000000
107	6B	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
108	6C	Detailed Timing Description #4	00	00000000
109	6D	Flags	00	00000000
110	6E	Reserved	00	00000000
111	6F	For Brightness Table and Power Consumption	02	00000010
112	70	Flags	00	00000000
113	71	PWM % [7:0] @ Step 0 = 5%	0C	00001100
114	72	PWM % [7:0] @ Step 5 = 20%	33	00110011
115	73	PWM % [7:0] @ Step 10 = 100%	FF	11111111
116	74	Nits [7:0] @ Step 0 = 15nits	0F	00001111
117	75	Nits [7:0] @ Step 5 = 60nits	3C	00111100
118	76	Nits [7:0] @ Step 10 = 300nits	96	10010110
119	77	Panel Electronics Power @32x32 Chess Pattern =2000mW	32	00110010
120	78	Backlight Power @60 nits =1380mW	22	00100010
121	79	Backlight Power @Step 10 =6900mW	56	01010110
122	7A	Nits @ 100% PWM Duty =300nit	96	10010110
123	7B	Flags	00	00000000
124	7C	Flags	00	00000000
125	7D	Flags	00	00000000
126	7E	Extension flag	00	00000000
127	7F	Checksum	2A	00101010

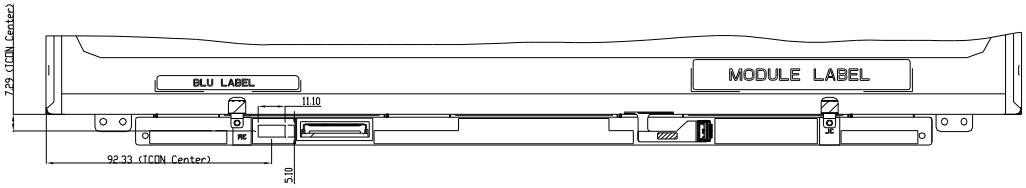
Appendix. OUTLINE DRAWING







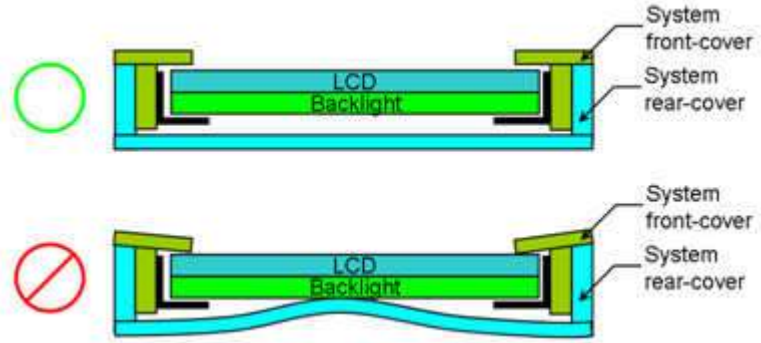
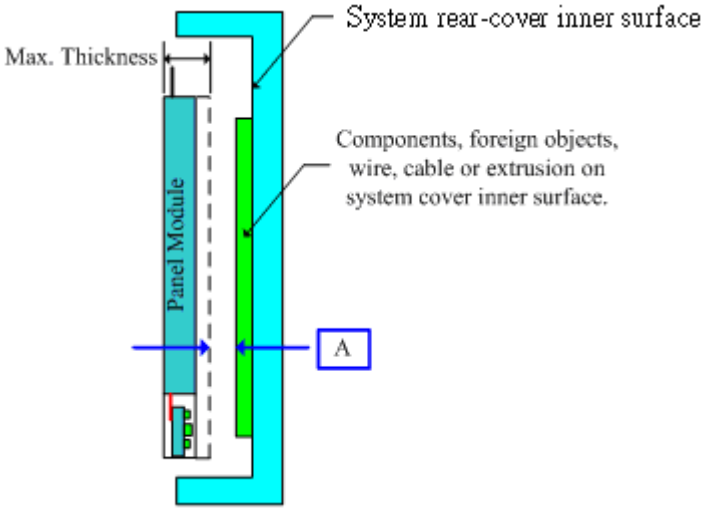


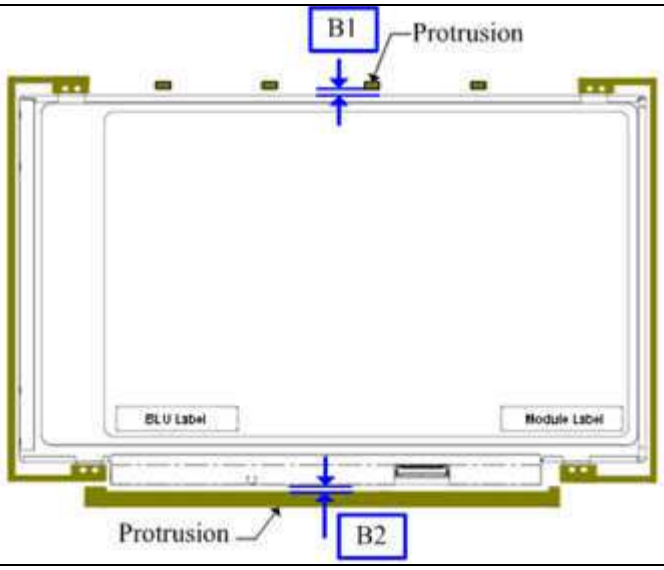


DRIVER IC, COF/FPC, AND TCON LOCATION
SEE NOTES FOR EXPLANATION

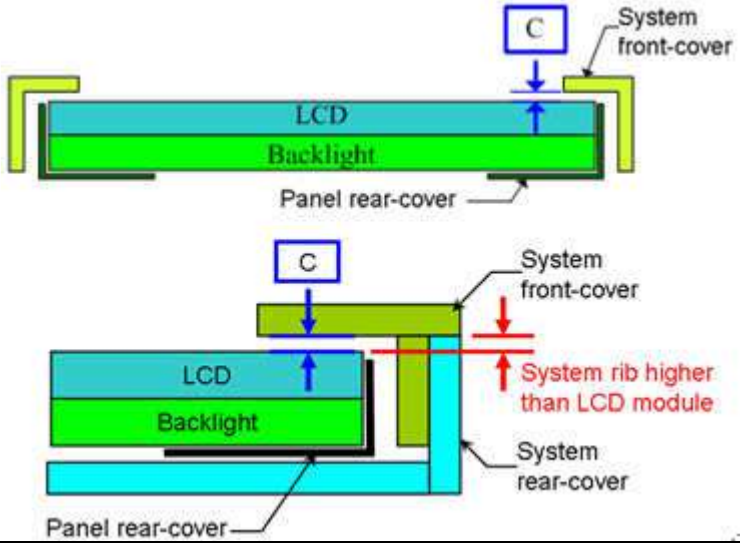
NOTES :
1. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR FOREIGN OBJECTS OVER FPC/COF, T-CON AND VR LOCATIONS.
2. LVDS/EDP CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
3. MODULE FLATNESS SPEC 0.5 mm MAX. (SPEC. WILL BE MODIFIED AFTER DVT CHECK).
4. "( )" MARKS THE REFERENCE DIMENSION.

Appendix. SYSTEM COVER DESIGN GUIDANCE Ver.7

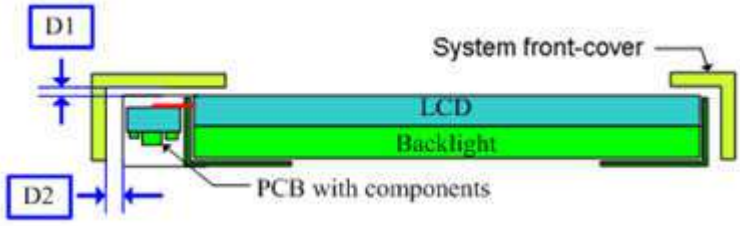
0.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1.	**Design gap A between panel & any components on system rear-cover**
	
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Maximum flatness of panel and system rear-cover should be taken into account for gap design. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
2	**Design gap B1 & B2 between panel & protrusions**



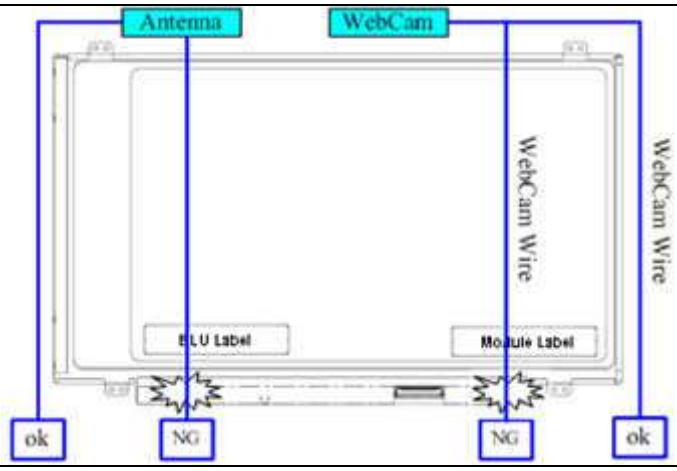
Definition	Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur. The gap should be large enough to absorb the maximum displacement during the test. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
3	**Design gap C between system front-cover & panel surface.**



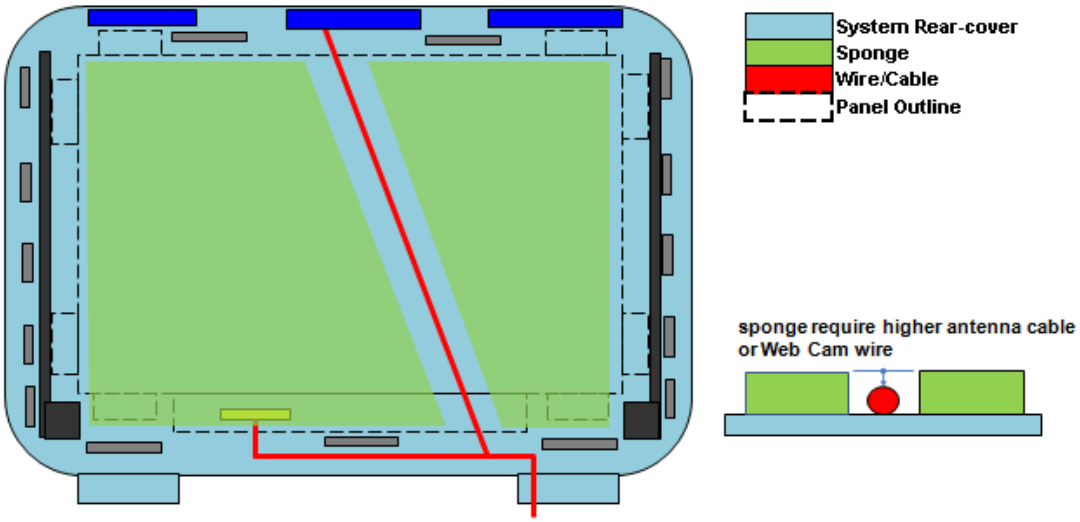
Definition	Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
4	**Design gap D1 & D2 between system front-cover & PCB Assembly.**



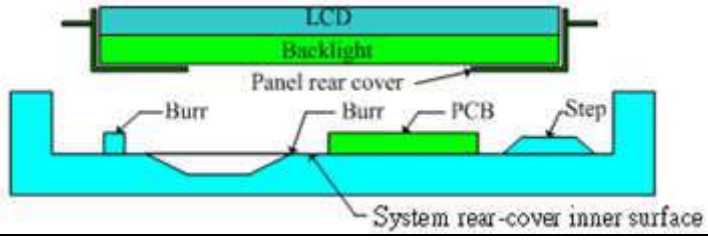
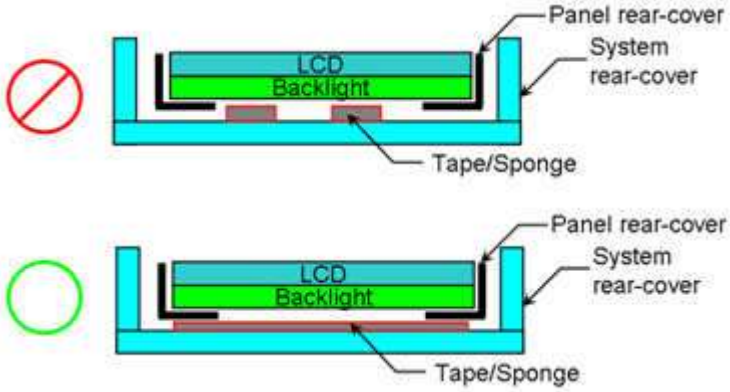
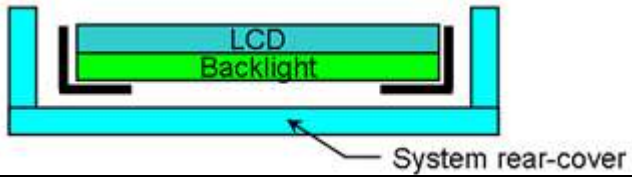
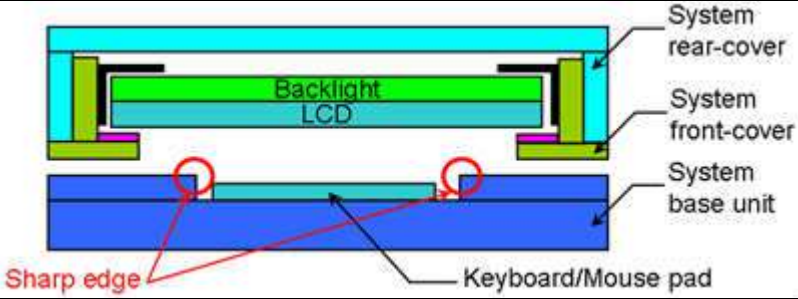
Definition	Same as point 2 and 3, but focus on PCBA side.
5	**Interference examination of antenna cable and WebCam wire**

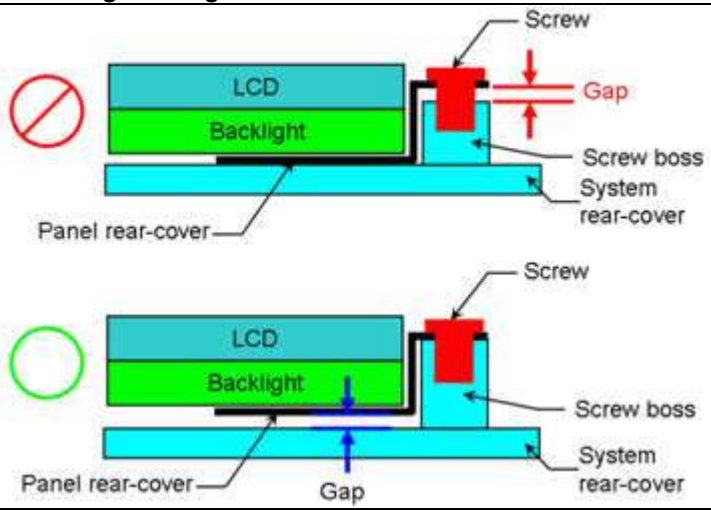
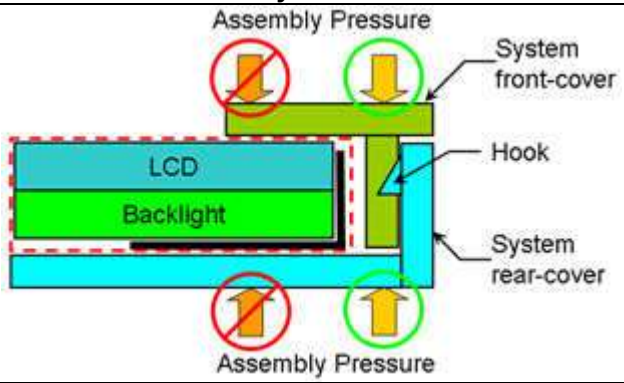
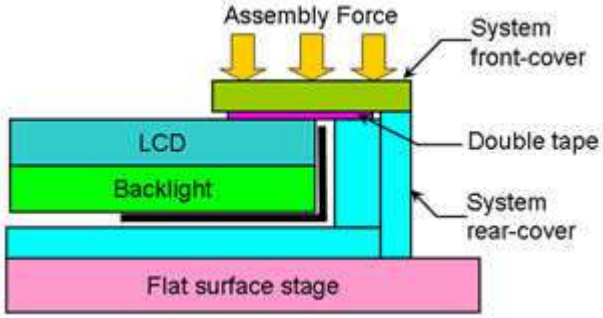


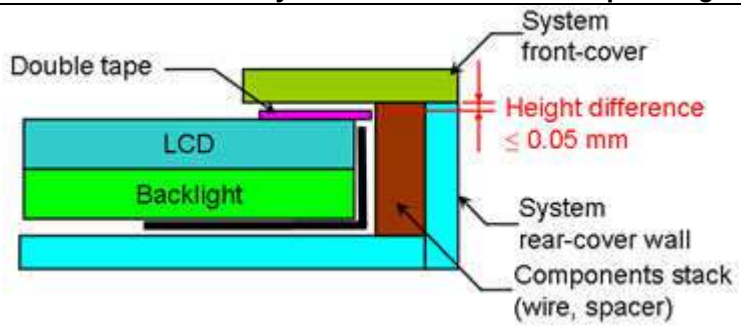
Definition	Antenna cable or WebCam wire should not overlap with panel outline. Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
6	**Interference examination of antenna cable and Web Cam wire**

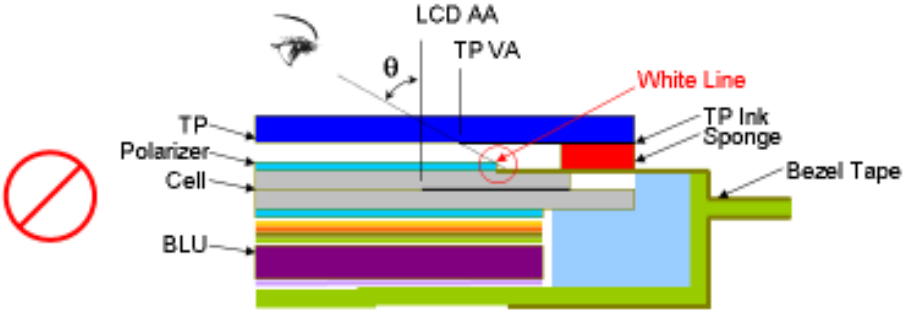


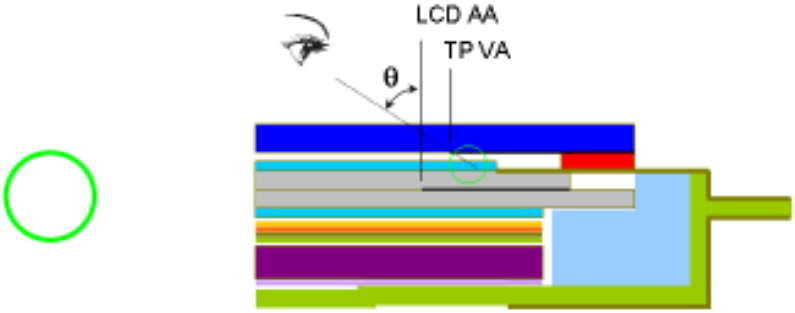
	If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.(Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC) Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

7	**System rear-cover inner surface examination**
	
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
8	**Tape/sponge design on system inner surface**
	
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.
9	**Material used for system rear-cover**
	
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
10	**System base unit design near keyboard and mouse pad**
	
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, sharp edge design in keyboard surface may damage panel during the test. We suggest to use slope edge design, or to reduce the thickness difference of keyboard/mouse pad from

	the nearby surface.
11	**Screw boss height design**
	
Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
12	**Assembly SOP examination for system front-cover with Hook design**
	
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
13	**Assembly SOP examination for system front-cover with Double tape design**
	
Definition	To prevent panel crack during system front-cover assembly process with double tape design, it is only allowed to give slight pressure (MAX 3 Kgf/50mm2) with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.

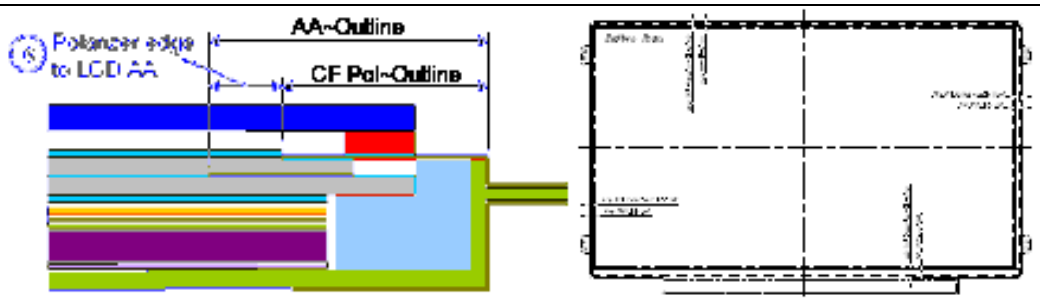
14	System front-cover assembly reference with Double tape design
	
Definition	To prevent system front-cover peeling at double tape contact area, Height difference between system front-cover assembly reference such as wall or components stack (wire, spacer) and double tape top surface must be less than 0.05mm.
15	**Touch Application : TP and LCD Module Combination for White Line Prevention**



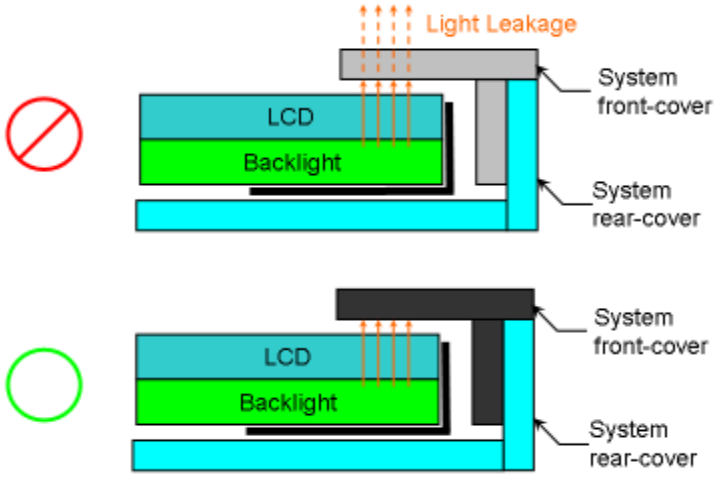


Parameter consideration for White Line Issue :	
1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection/Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

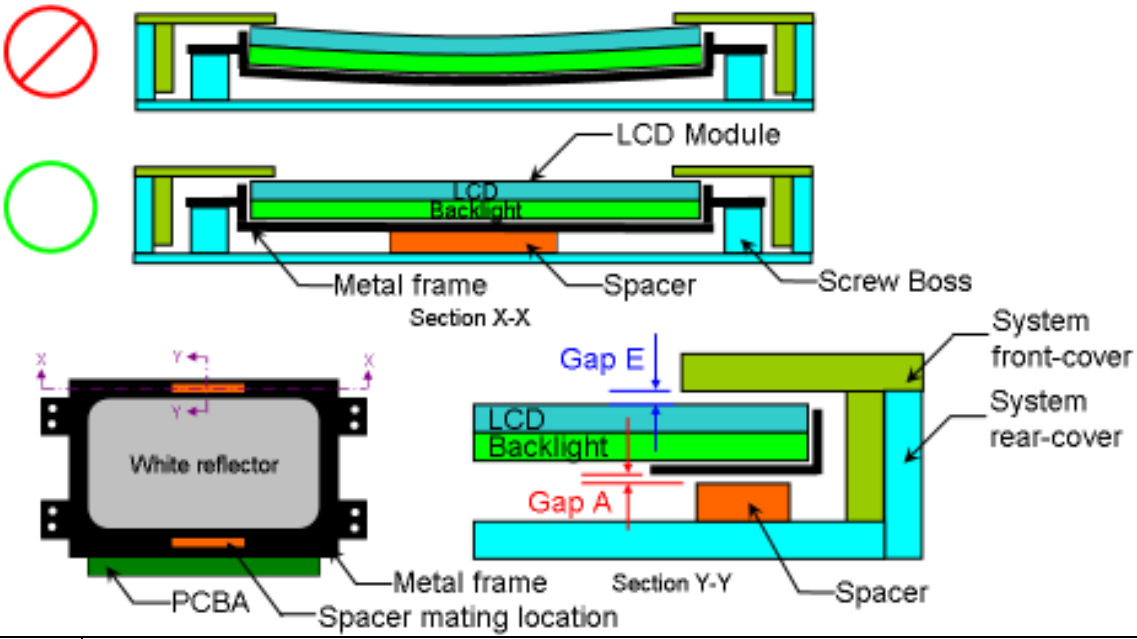
Polarizer edge to LCD AA distance can be derived by “AA~Outline” – “CF Pol~Outline” with respect to INX 2D Outline Drawing on each side.



Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module's Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing ("AA ~Outline" - "CF Pol~Outline"). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference.
16	**Color of system front-cover material**



Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.
17	**Inspection spec of gap E between system front-cover to LCD module surface**



Definition	To maintain gap E (gap of system front-cover to LCD module) in its inspection spec, especially at location with maximum LCD deformation (center of LCD length), we recommend adding spacer with design gap A smaller or equal to gap E. The allowable spacer mating location is on module metal frame outside LCD Active-Area. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

Appendix. LCD MODULE HANDLING MANUAL

Purpose	• **This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure.** • **This manual provides guide in unpacking and handling steps.** • **Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.**
1.	**Unpacking**
	
2.	**Panel Lifting**

Use slots at both sides for finger insertion.
Handle panel upward with care.

3.	Do and Don't

Do :

- Handle with both hands.
- Handle panel at left and right edge.

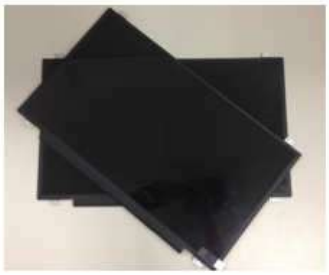
Don't :

- Lifting with one hand.

- Handle at PCBA side.

Don't :

- Stack panels.



- Press panel.

Don't :

- Put foreign stuff onto panel

- Put foreign stuff under panel

Don't :

- Paste any material unto white reflector sheet

Don't :

- Pull / Push white reflector sheet

Don't :

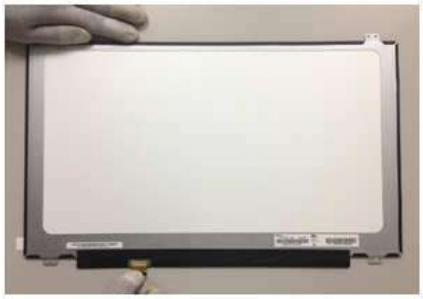
- Hold at panel corner.

Don't :

- Twist panel.

Do :

- Hold panel at top edge while inserting connector.



Don't :

- Press white reflector sheet while inserting connector.

Do :

- Remove panel protector film starts from pull tape

Don't :

- Remove panel protector film From film another side.

Don't :

- Touch or Press PCBA Area.